

03-24-j3 11:47am From-MORRISON & FOERSTER LLP

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T-243 P.002/004 F-698

Delaware

PAGE 1

The First State

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THE ATTACHED IS A TRUE AND CORRECT COPY OF THE CERTIFICATE OF INCORPORATION OF "PTS CORPORATION", FILED IN THIS OFFICE ON THE TWENTIETH DAY OF MARCH, A.D. 2003, AT 5 O'CLOCK P.M.

A FILED COPY OF THIS CERTIFICATE HAS BEEN FORWARDED TO THE NEW CASTLE COUNTY RECORDER OF DEEDS.



Harriet Smith Windsor
Harriet Smith Windsor, Secretary of State

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AUTHENTICATION: 2325435

J3-24-3

11:47am From-MORRISON & FERNSTER LLP

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STATE OF DELAWARE
SECRETARY OF STATE
DIVISION OF CORPORATIONS
FILED 05:00 PM 03/20/2003
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CERTIFICATE OF INCORPORATION
OF
PTS CORPORATION

1. The name of the corporation is PTS Corporation (the "Corporation").
2. The address of the corporation's registered office in the State of Delaware is 2711 Centerville Road, Suite 400, in the City of Wilmington, 19808, County of New Castle. The name of its registered agent at such address is Corporation Service Company.
3. The nature of the business of the Corporation and the objects or purposes to be transacted, promoted or carried on by it are as follows: To engage in any lawful act or activity for which corporations may be organized under the General Corporation Law of the State of Delaware.
4. The total number of shares of all classes of stock that the Corporation is authorized to issue is One Thousand (1,000) shares of Common Stock with a par value of \$0.001 per share.
5. The Board of Directors is expressly authorized to make, alter or repeal the Bylaws of the Corporation.
6. Elections of directors need not be by written ballot unless the Bylaws of the Corporation shall so provide.
7. Whenever a compromise or arrangement is proposed between this Corporation and its creditors or any class of them and/or between this Corporation and its stockholders or any class of them, any court of equitable jurisdiction within the State of Delaware may, on the application in a summary way of this Corporation or of any creditor or stockholder thereof, or on the application of any receiver or receivers appointed for this Corporation under the provisions of Section 291 of Title 8 of the Delaware Code or on the application of trustees in dissolution or of any receiver or receivers appointed for this Corporation under the provisions of Section 279 of Title 8 of the Delaware Code order a meeting of the creditors or class of creditors, and/or of the stockholders or class of stockholders of this Corporation, as the case may be, to be summoned in such manner as the said court directs. If a majority in number representing three-fourths in value of the creditors or class of creditors, and/or of the stockholders or class of stockholders of this Corporation, as the case may be, agree to any compromise or arrangement and to any reorganization of this Corporation as a consequence of such compromise or arrangement, the said compromise or arrangement and the said reorganization shall, if sanctioned by the court to which the said application has been made, be binding on all the creditors or class of creditors, and/or on all the stockholders or class of stockholders, of this Corporation, as the case may be, and also on this Corporation.
8. The Corporation reserves the right to amend, alter, change or repeal any provision contained in this Certificate of Incorporation, in the manner now or hereafter prescribed by statute, and all rights conferred upon stockholders herein are granted subject to this reservation.

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9. To the fullest extent permitted by Delaware statutory or decisional law, as amended or interpreted, no director of this Corporation shall be personally liable to the Corporation or its stockholders for monetary damages in excess of One Dollar (\$1.00) per director per occurrence for breach of fiduciary duty as a director. This Article 9 does not affect the availability of equitable remedies for breach of fiduciary duties.

10. The name and mailing address of the sole incorporator is as follows:

| Name | Mailing Address |
|-------------------|--|
| Brian Lewandowski | c/o Morrison & Foerster LLP 5200 Republic Plaza 370 17th Street Denver, Colorado 80202-5638 |

I, the undersigned, being the sole incorporator hereinbefore named, for the purpose of forming a corporation pursuant to the General Corporation Law of the State of Delaware, do make this certificate, hereby declaring and certifying that this is my act and deed and the facts herein stated are true, and, accordingly, have hereunto set my hands this 19th day of March, 2003.

/s/ Brian D. Lewandowski
Brian Lewandowski, Sole Incorporator

Exhibit A

ASSIGNMENT AND TRANSFER OF PATENTS

WHEREAS, BOPS, Inc., a Delaware corporation, with offices at 1200 Charleston Road, Mountain View, California 94043 ("Assignor") owns certain patent applications and/or registrations, as listed in Exhibit A attached hereto and incorporated herein by this reference ("Patents"); and

WHEREAS, Altera Corporation, a Delaware corporation, with offices at 101 Innovation Drive, San Jose, California 95134 ("Assignee"), desires to acquire all of the right, title and interest of Assignor in, to and under the Patents;

WHEREAS, Assignor and Assignee have entered into a certain Asset Purchase Agreement, dated as of December 20, 2002 ("Assignment Agreement"), assigning, among other things, all right, title and interest in and to the Patents and in and to the registrations for same from Assignor to Assignee;

NOW, THEREFORE, for good and valuable consideration described in the Assignment Agreement, the receipt and sufficiency of which are hereby acknowledged, Assignor does hereby irrevocably sell, assign, transfer and convey unto Assignee all of its right, title and interest in and to the Patents, including all divisions, continuations-in-part, reexaminations, substitutions, reissues, extensions and renewals of the applications and registrations for the Patents (and the right to apply for any of the foregoing); all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the Patents throughout the universe, including without limitation all foreign counterparts and foreign equivalents of any of the foregoing.

Assignor authorizes and requests the patent officials in the United States and in any and all foreign jurisdictions to issue any and all letters patent and foreign counterparts or equivalents thereof to Altera Corporation, as assignee of the entire interest of Assignor therein, and covenants that Assignor has full right to convey the entire interest herein assigned and that Assignor has not executed and will not execute any agreements in conflict herewith.

Assignor further agrees, for itself, its successors and assigns, to execute such further documents and to perform such further lawful acts as may reasonably be required to effectuate this assignment.

IN WITNESS WHEREOF, Assignor has caused this assignment to be duly executed by an authorized officer on this 20th day of December, 2002.

BOPS, INC.

By: Carl Schlachte

Carl Schlachte
Chairman and Chief Executive Officer

STATE OF CALIFORNIA)

COUNTY OF San Mateo) ss.

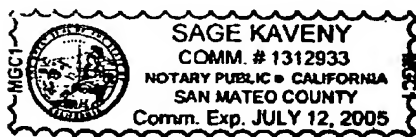
On December 20, 2002, before me, the undersigned notary public in and for said County and State, personally appeared Carl Schlachte Jr.

 personally known to me [or]

✓ proved to me on the basis of satisfactory evidence

to be the person(s) whose name(s) is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity(ies) and that, by his signature(s) on the instrument, the person(s) or the entity(ies) upon behalf of which the person(s) acted executed the instrument.

Witness my hand and official seal.



Sage Kaveny
My commission expires on
7/12/05

EXHIBIT A **PATENTS**

| Client No. | Title | Country. | Inventors | Application No. |
|--------------|--|-------------------|---|-----------------|
| | Filing Date | Patent No. | | |
| 800.0001 | Manifold Array Processor 6/30/1997 | U.S. 6,023,753 | Pechanek, G | 08/885,310 ✓ |
| 800.0001-PCT | Manifold Array Processor 6/24/1998 | PCT | Kurak, Jr., | PCT/US98/13111 |
| 800.0001-EP | Manifold Array Processor 6/24/1998 | EP 1002279 | | 98932831.5-2201 |
| 800.0001-CA | Manifold Array Processor 6/24/1998 | CA | | 2,295,109 |
| 800.0001-CN | Manifold Array Processor 6/24/1998 | CN | | 98806757.9 |
| 800.0001-IL | Manifold Array Processor 6/24/1998 | IL | | 133,691 |
| 800.0001-JP | Manifold Array Processor 6/24/1998 | JP | | 11-505670 |
| 800.0001-KR | Manifold Array Processor 6/24/1998 | KR | | 10-1999-7012547 |
| 800.0001-MX | Manifold Array Processor 6/24/1998 | MX | | 09911982 |
| 800.0002 | Method and Apparatus for 10/10/1997 Manifold Array Processing | U.S. 6,167,502 | Pechanek, G | 08/949,122 |
| 800.0002-PCT | Method and Apparatus for 10/9/1998 Manifold Array Processing | PCT | Pitsianis, N Barry, E | PCT/US98/21478 |
| 800.0002-EP | Method and Apparatus for 10/9/1998 | EP 1034484 | | 98954956.3 |
| 800.0002-CA | Method and Apparatus for 10/9/1998 | CA | | 2,305,221 |
| 800.0002-CN | Method and Apparatus for 10/9/1998 | CN | | 98809446.0 |
| 800.0002-IL | Method and Apparatus for 10/9/1998 | IL | | 135,535 |
| 800.0002-JP | Method and Apparatus for 10/9/1998 | JP | | 2000-516291 |
| 800.0002-KR | Method and Apparatus for 10/9/1998 | KR | | 10-2000-7003864 |
| 800.0002-MX | Method and Apparatus for 10/9/1998 Manifold Array Processing | MX | | 3003 |
| 800.0004 | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | U.S. 6,151,668 | Pechanek, G Drabenstott, Revilla, J | 09/187,539 |

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|---------------|--|-------------------|---|-----------------|
| 800.0004-PCT | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | PCT | | PCT/US98/23650 |
| 800.0004-EP | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | EP 1029266 | | 98957630.1 |
| 800.0004-CA | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | CA | | 2,310,584 |
| 800.0004-CN | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | CN | | 98810767.8 |
| 800.0004-IL | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | IL | | 135,953 |
| 800.0004-JP | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | JP | | 2000-51983 |
| 800.0004-KR | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | KR | | 10-2000-7004975 |
| 800.0004-MX | Methods and Apparatus for 11/6/1998 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | MX | | 3803 |
| 800.0004.PROV | Methods and Apparatus for 11/7/1997 Efficient Synchronous MIMD VLIW Communication | U.S. | Pechanek, G Drabenstott, Revilla, J | 60/064,619 |
| 800.0011 | Methods and Apparatus for 10/9/1998 Dynamic Instruction Controlled Reconfiguration Reg | U.S. 6,343,356 | Pechanek, G Barry, E | 09/169,255 |
| 800.0011.PROV | Methods and Apparatus for 7/9/1998 Dynamic Instruction Controlled Reconfiguration Reg | U.S. | Pechanek, G Barry, E | 60/092,148 |
| 800.0012 | Methods and Apparatus for 10/9/1998 ManArray PE-PE Switch Control | U.S. 6,167,501 | Barry, E Pechanek, G Drabenstott, | 09/169,256 |
| 800.0012-PCT | Methods and Apparatus for 10/8/1999 ManArray PE-PE Switch Control | PCT | | PCT/US99/23493 |
| 800.0012-EP | Methods and Apparatus for 10/8/1999 ManArray PE-PE Switch Control | EP 1137999 | | 99953107.2 |
| 800.0012-JP | Methods and Apparatus for 10/8/1999 ManArray PE-PE Switch Control | JP | | 2000-576380 |

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|---------------|---|-------------------|---|----------------|
| 800.0012.PROV | Methods and Apparatus for 6/5/1998 ManArray PE-PE Switch Control | U.S. | Barry, E Pechanek, G Drabenstott, | 60/088,148 |
| 800.0013 | Methods and Apparatus for 12/18/1998 Scalable Instruction Set Architecture with Dynamic Comp | U.S. 6,101,592 | Pechanek, G Barry, E Revilla, J | 09/215,081 |
| 800.0013-PCT | Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp | PCT | | PCT/US99/29516 |
| 800.0013-EP | Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp | EP | | 99968117.4 |
| 800.0013-IL | Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp | IL | | 143,431 |
| 800.0013-JP | Methods and Apparatus for 12/14/1999 Scalable Instruction Set Architecture with Dynamic Comp | JP | | 2000-590073 |
| 800.0013.PROV | Methods and Apparatus for 12/18/1997 Scalable Instruction Set Architecture | U.S. | Pechanek, G Barry, E Drabenstott, | 60/068,021 |
| 800.0016 | Methods and Apparatus for 12/4/1998 Dynamic Very Long Instruction Word Sub-Instruction Selection | U.S. 6,173,389 | Pechanek, G Revilla, J Barry, E | 09/205,588 |
| 800.0016-PCT | System for Dynamic VLIW 12/2/1999 Sub-Instruction Selection for Execution Time Parallelism in | PCT | | PCT/US99/28506 |
| 800.0016-EP | System for Dynamic VLIW 12/2/1999 Sub-Instruction Selection for Execution Time Parallelism in | EP 1247196 | | 99965084.9 |
| 800.0016-JP | System for Dynamic VLIW 12/2/1999 Sub-Instruction Selection for Execution Time Parallelism in | JP | | 2000-596762 |
| 800.0016-IL | System for Dynamic VLIW 12/2/1999 Sub-Instruction Selection for Execution Time Parallelism in | IL | | 143,430 |
| 800.0016.PROV | Method and Apparatus for 12/4/1997 Dynamically Modifying Instructions in a Very Long In | U.S. | Revilla, J Barry, E Pechanek, G | 60/067,511 |
| 800.0017 | Methods and Apparatus to 1/12/1999 Dynamically Reconfigure the Instruction Pipeline of an Ind | U.S. 6,216,223 | Revilla, J Barry, E Marchand, P | 09/228,374 |

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|---------------|--|-------------------|---|-----------------|
| 800.0017-PCT | Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of Indire | PCT | | PCT/US00/00569 |
| 800.0017-EP | Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of an Ind | EP | | 00903213.7-2201 |
| 800.0017-IL | Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of an Ind | IL | | 144,162 |
| 800.0017-JP | Methods and Apparatus to 1/10/2000 Dynamically Reconfigure the Instruction Pipeline of an Ind | JP | | 2000-594009 |
| 800.0017.PROV | Methods and Apparatus to 1/12/1998 Dynamically Expand the Instruction Pipeline of a Very | U.S. | Revilla, J | 60/071,248 |
| 800.0021 | Methods and Apparatus to 1/28/1999 Support Conditional Execution in a VLIW-Based Array Processo | U.S. 6,366,999 | Drabenstott, Pechanek, G | 09/238,446 |
| 800.0021-PCT | Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo | PCT | Barry, E | PCT/US00/01803 |
| 800.0021-EP | Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo | EP 1196855 | | 00911637.7 |
| 800.0021-IL | Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo | IL | | 144,562 |
| 800.0021-JP | Methods and Apparatus to 1/24/2000 Support Conditional Execution in a VLIW-Based Array Processo | JP | | 2000-596471 |
| 800.0021.PROV | Methods and Apparatus to 1/28/1998 Support Conditional Execution in a VLIW-Based Array Processo | U.S. | Drabenstott, Pechanek, G Revilla, J | 60/072,915 |
| 800.0022 | Merged Array Controller with 10/9/1998 Processing Element | U.S. 6,219,776 | Pechanek, G | 09/169,072 |
| 800.0022-PCT | Methods and Apparatus for 10/8/1999 Dynamically Merging an Array Controller with an Array Proce | PCT | Revilla, J | PCT/US99/23495 |
| 800.0022-EP | Methods and Apparatus for 10/8/1999 Dynamically Merging an Array Controller with an Array Proce | EP 1127316 | | 99953109.8 |
| 800.0022-JP | Methods and Apparatus for 10/8/1999 Dynamically Merging an Array | JP | | 2000-576374 |

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|---------------|--|-------------------|--|----------------|
| | Controller with an Array Proce | | | |
| 800.0022.PROV | Methods and Apparatus for 3/10/1998 Dynamically Merging an Array Controller with an Array Proce | U.S. | Pechanek, G Revilla, J | 60/077,457 |
| 800.0023 | Register File Indexing 3/12/1999 | U.S. 6,446,190 | Barry, E | 09/267,570 |
| 800.0023-PCT | Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000 | PCT | Pechanek, G Marchand, P | PCT/US00/06334 |
| 800.0023-EP | Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000 | EP | | 00913887.6 |
| 800.0023-CA | Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000 | CA | | |
| 800.0023-IL | Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000 | IL | | 144,970 |
| 800.0023-JP | Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/9/2000 | JP | | 2000-604303 |
| 8 0.0023.PROV | Methods and Apparatus for Providing Indirect Control of Register File Indexing 3/12/1998 | U.S. | Barry, E | 60/077,766 |
| 800.0024 | Accessing Tables in Memory 6/16/2000 | U.S. 6,397,324 | Barry, E | 09/596,103 |
| 800.0024-PCT | Banks Using Load and Store Address Generators Sharing Sto Methods and Apparatus for 5/10/2001 | PCT | Kurak, Jr., Pechanek, G | PCT/US01/15232 |
| 800.0024-EP | Data Dependent Address Operations and Efficient Varia Methods and Apparatus for 5/10/2001 | EP | | 01935327.5 |
| 800.0024.PROV | Data Dependent Address Operations and Efficient Varia Methods and Apparatus for 6/18/1999 | U.S. | Barry, E Kurak, Jr., Pechanek, G | 60/139,946 |
| 800.0025 | Generalized Event Detection and Action Specification in a Methods and Apparatus for 6/21/2000 | U.S. | Barry, E | 09/598,566 |
| 800.0025-PCT | Generalized Event Detection Methods and Apparatus for 6/21/2000 | PCT | Marchand, P Pechanek, G | PCT/US00/40273 |

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| 800.0025-EP | and Action Specification in a Methods and Apparatus for 6/21/2000 Generalized Event Detection and Action Specification in a | EP | | 00955904.8 |
| 800.0025.PROV | Methods and Apparatus for 6/21/1999 Generalized Event Detection and Action Specification in a | U.S. | Barry, E Marchand, P Pechanek, G | 60/140,245 |
| 800.0026 | Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding | U.S. | Kurak, Jr., Moller, C | 09/432,705 |
| 800.0026-PCT | Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding | PCT | | PCT/US99/25707 |
| 800.0026-EP | Improved Motion Estimation 11/2/1999 | EP 1157559 | | 99971615.2 |
| 800.0026-JP | Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding | JP | | 2000-580388 |
| 800.0026-IL | Methods and Apparatus for 11/2/1999 Improved Motion Estimation for Video Encoding | IL | | 142,856 |
| 800.0026.PROV | Methods and Apparatus for 11/3/1998 Improved Motion Estimation for Video Encoding | U.S. | | 60/106,867 |
| 800.0027 | Methods and Apparatus for 7/9/1999 Instruction Addressing in Indirect VLIW Processors | U.S. 6,356,994 | Barry, E Pechanek, G | 09/350,191 |
| 800.0027-PCT | Methods and Apparatus for 7/7/2000 Instruction Addressing in Indirect VLIW Processors | PCT | | PCT/US00/40143 |
| 800.0027-EP | Methods and Apparatus for 6/7/2000 Instruction Addressing in Indirect VLIW Processors | EP | | 00943442.4 |
| 800.0027.PROV | Methods and Apparatus for 7/9/1998 Instruction Addressing in Indirect VLIW Processors | U.S. | Barry, E | 60/092,130 |
| 800.0028 | Methods and Apparatus for 12/22/2000 Loading a Very Long Instruction Word Memory | U.S. | Barry, E Pechanek, G | 09/747,056 |
| 800.0028.PROV | Methods and Apparatus for 12/23/1999 Loading a Very Long Instruction Word Memory | U.S. | Barry, E Pechanek, G | 60/171,911 |

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| 800.0029 | Efficient Complex 6/22/1999 | U.S. | Pitsianis, N | 09/337,839 |
| 800.0029-PCT | Multiplication and Fast Fourier Transform (FFT) Implem Efficient Complex 10/8/1999 | PCT | Pechanek, G Rodriguez, R | PCT/US99/23494 |
| 800.0029-EP | Multiplication and Fast Fourier Transform (FFT) Implem Efficient Complex 10/8/1999 | EP 1141819 | | 99953108.0 |
| 800.0029-JP | Multiplication and Fast Fourier Transform (FFT) Implem Efficient Complex 10/8/1999 | JP | | 2000-576342 |
| 800.0029.CPA | Multiplication and Fast Fourier Transform (FFT) Implem Efficient Complex 6/22/1999 | U.S. | Pitsianis, N | 09/337,839 |
| 800.0029.PROV | Multiplication and Fast Fourier Transform (FFT) Implem Efficient Complex 10/9/1998 | U.S. | Pitsianis, N | 60/103,712 |
| 800.0030 | Methods and Apparatus for 12/23/1999 | U.S. 6,256,683 | Barry, E | 09/472,372 |
| 800.0030-PCT | Providing Direct Memory Access Control Methods and Apparatus for 12/19/2000 | PCT | | PCT/US00/34456 |
| 800.0030-EP | Providing Direct Memory Access Control Methods and Apparatus for 12/19/2000 | EP | | 00986567.6 |
| 800.0030.PROV | Providing Direct Memory Access Control Methods and Apparatus for 12/23/1998 | U.S. | Barry, E | 60/113,637 |
| 800.0031 | Providing Data Transfer Methods and Apparatus for 12/19/2000 | U.S. 6,260,082 | Barry, E | 09/471,217 |
| 800.0031-PCT | Providing Data Transfer Methods and Apparatus for 12/19/2000 | PCT | Wolff, E | PCT/US00/34454 |
| 800.0031-EP | Providing Data Transfer Methods and Apparatus for 12/19/2000 | EP | | 00988150.9 |
| 800.0031.PROV | Providing Data Transfer Methods and Apparatus 12/23/1998 | U.S. | Barry, E | 60/113,555 |
| 800.0032 | Providing Transfer Control Manifold Array Processor 6/1/1999 | U.S. 6,338,129 | Pechanek, G | 09/323,609 |

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| 800.0034 | Methods and Apparatus for 6/22/2000 Parallel Processing Utilizing a Manifold Array (ManArray) Ar | U.S. | Kurak, Jr., Pechanek, G | 09/599,980 |
| 800.0034.PROV | Methods and Apparatus for 6/22/1999 Parallel Processing Utilizing a Manifold Array (ManArray) Ar | U.S. | Strube, D Barry, E | 60/140,425 |
| 800.0035 | Methods and Apparatus for 6/21/2000 Improved Efficiency in Pipeline Simulation and Emulat | U.S. | Moller, C | 09/598,567 |
| 800.0035.PROV | Methods and Apparatus for 6/21/1999 Improved Efficiency in Pipeline Simulation and Emulat | U.S. | Busboom, C Schneider, D | 60/140,163 |
| 800.0036 | Methods and Apparatus for 6/21/2000 Initiating and Resynchronizing Multi-Cycle SI | U.S. | Pechanek, G | 09/598,564 |
| 800.0036-PCT | Methods and Apparatus for 6/21/2000 Initiating and Resynchronizing Multi-Cycle SI | PCT | Strube, D Wolff, E | PCT/US00/40283 |
| 800.0036-EP | Methods and Apparatus for 6/21/2000 Initiating and Resynchronizing Multi-Cycle SI | EP | | 00960114.7 |
| 800.0036.PROV | Methods and Apparatus for 6/21/1999 Initiating and Resynchronizing Multi-Cycle SI | U.S. | Pechanek, G | 60/140,162 |
| 800.0037 | Methods and Apparatus for 6/21/2000 Providing Manifold Array (ManArray) Program Context Swi | U.S. | Strube, D Morris, G | 09/598,558 |
| 800.0037-PCT | Methods and Apparatus for 6/21/2000 Providing Manifold Array (ManArray) Program Context Swi | PCT | Barry, E | PCT/US00/40272 |
| 800.0037-EP | Methods and Apparatus for 6/21/2000 Providing Manifold Array (ManArray) Program Context Swi | EP | Pechanek, G Strube, D | 00955903.0 |
| 800.0037.PROV | Methods and Apparatus for 6/21/1999 Providing One-by-One Manifold Array (1x1 ManArray) Program C | U.S. | Barry, E | 60/140,244 |
| 800.0038 | Methods and Apparatus for 6/21/2000 Establishing Port Priority Functions in a VLIW Processor | U.S. | Strube, D | 09/598,084 |
| | | | Barry, E | |
| | | | Wolff, E Marchand, P | |

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| 800.0038-PCT | Methods and Apparatus for 6/21/2000 Establishing Port Priority Functions in a VLIW Processor | PCT | | PCT/US00/40263 |
| 800.0038-EP | Methods and Apparatus for 6/21/2000 Establishing Port Priority Functions in a VLIW Processor | EP | | 00951075.1 |
| 800.0038.PROV | Methods and Apparatus for 6/21/1999 Establishing Port Priority Functions in a VLIW Processor | U.S. | Barry, E | 60/140,325 |
| 800.0039 | Methods and Apparatus for 10/21/1999 Abbreviated Instruction Sets Adaptable to Configurable Proc | U.S. 6,408,382 | Pechanek, G | 09/422,015 |
| 800.0039-PCT | Methods and Apparatus for 10/16/2000 Abbreviated Instruction and Configurable Processor Archite | PCT | Kurak, Jr., Larsen, L | PCT/US00/28622 |
| 800.0039-EP | Methods and Apparatus for 10/16/2000 Abbreviated Instruction and Configurable Processor Archite | EP | | 00970952.8 |
| 800.0040 | Methods and Apparatus for 11/9/2000 Efficient Cosine Transform Implementations | U.S. | Kurak, Jr., Pechanek, G | 09/711,218 |
| 800.0040-PCT | Methods and Apparatus for 11/9/2000 Efficient Cosine Transform Implementations | PCT | | PCT/US00/31120 |
| 800.0040-EP | Methods and Apparatus for 11/9/2000 Efficient Cosine Transform Implementations | EP | | 00977189.0 |
| 800.0040.PROV | Methods and Apparatus for 11/12/1999 Efficient Cosine Transform Implementations | U.S. | Kurak, Jr., Pechanek, G | 60/165,337 |
| 800.0042 | Methods and Apparatus for 2/23/2001 Providing Bit-Reversal and Multicast Functions Utilizing | U.S. | Barry, E | 09/791,940 |
| 800.0042-PCT | Methods and Apparatus for 2/23/2001 Providing Bit-Reversal and Multicast Functions Utilizing | PCT | Pitsianis, N Coopman, K | PCT/US01/05714 |
| 800.0042-EP | Methods and Apparatus for 2/23/2001 Providing Bit-Reversal and Multicast Functions Utilizing | EP | | 01912939.4 |
| 800.0042.PROV | Methods and Apparatus for 2/24/2000 Providing Bit-Reversal and Multicast Functions Utilizing | U.S. | Barry, E Pitsianis, N Coopman, K | 60/184,668 |

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| 800.0043 | Methods and Apparatus for 2/23/2001 Scalable Array Processor Interrupt Detection and Respon | U.S. | Barry, E | 09/791,256 |
| 800.0043-PCT | Methods and Apparatus for 2/23/2001 Scalable Array Processor Interrupt Detection and Respon | PCT | Marchand, P Pechanek, G | PCT/US01/06058 |
| 800.0043-EP | Methods and Apparatus for 2/23/2001 Scalable Array Processor Interrupt Detection and Respon | EP | | 01916233.8 |
| 800.0043.PROV | Methods and Apparatus for 2/24/2000 Scalable Array Processor Interrupt Detection and Respon | U.S. | Barry, E | 60/184,529 |
| 800.0044 | Methods and Apparatus for 2/23/2001 Dual-Use Coprocessing/Debug Interface | U.S. | Barry, E | 09/792,819 |
| 800.0044-PCT | Methods and Apparatus for 2/23/2001 Dual-Use Coprocessing/Debug Interface | PCT | | PCT/US01/06004 |
| 800.0044-EP | Methods and Apparatus for 2/23/2001 Dual-Use Coprocessing/Debug Interface | EP | | 01914486.4 |
| 800.0044.PROV | Methods and Apparatus for 2/24/2000 Flexible Strength Coprocessing Interface | U.S. | Barry, E | 60/184,560 |
| 800.0045.PROV | Efficient Transformation and 3/29/2002 Lighting Implementation for 3D Graphics | U.S. | Rodriguez, R Jacobs, M Strube, D | 60/368,509 |
| 800.0046 | Methods and Apparatus for 11/1/2001 Efficient Complex Long Multiplication and Covariance | U.S. | Pechanek, G | 10/004,010 |
| 800.0046-PCT | Methods and Apparatus for 11/1/2001 Efficient Complex Long Multiplication and Covariance | PCT | Rodriguez, R Plonski, M | PCT/US01/45172 |
| 800.0046-EP | Methods and Apparatus for Efficient Complex Long Multiplication and Covariance | EP | | 01992935.5 |
| 800.0046.PROV | Methods and Apparatus for 11/1/2000 Efficient Complex Long Multiplication and Covariance | U.S. | Pechanek, G | 60/244,861 |
| 800.0049 | Methods and Apparatus for 4/5/2000 Scalable Instruction Set | U.S. 6,321,322 | Pechanek, G Barry, E | 09/543,473 |

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| | Architecture with Dynamic Comp | | Revilla, J | |
| 800.0052 | Methods and Apparatus for 5/11/2001 Power Control in a Scalable Array of Processor Elements | U.S. | Marchand, P Pechanek, G Wolff, E | 09/853,989 |
| 800.0052.PROV | Methods and Apparatus for 5/12/2000 Power Control in a Scalable Array of Processor Elements | U.S. | Marchand, P Pechanek, G Wolff, E | 60/203,629 |
| 800.0053 | Methods and Apparatus for 6/21/2001 Indirect VLIW Memory | U.S. | Pitsianis, N Strautin, B Banerjee, S | 09/886,855 |
| 800.0053.PCT | Methods and Apparatus for 6/21/2001 Indirect VLIW Memory | PCT | | PCT/US01/19851 |
| 800.0053-EP | Methods and Apparatus for 6/21/2001 Indirect VLIW Memory | EP | | 01946628.3 |
| 800.0053.PROV | Methods and Apparatus for 6/21/2000 Indirect VLIW Memory | U.S. | Pitsianis, N Strautin, B Banerjee, S | 60/212,987 |
| 800.0057 | Methods and Apparatus for 4/4/2002 Generating Functional Test Programs by Traversing a Finit | U.S. | Raimi, R Aloul, F | 10/116,221 |
| 800.0057.PROV | Methods and Apparatus for 4/4/2001 Generating Functional Test Programs by Traversing a Finit | U.S. | Raimi, R Aloul, F | 60/281,523 |
| 800.0066 | Methods and Apparatus for 8/29/2000 ManArray PE-PE Switch Control | U.S. 6,366,997 | Barry, E Pechanek, G Drabenstott, | 09/649,647 |
| 800.0067 | Methods and Apparatus for 10/2/2000 Efficient Synchronous MIMD Operations with iVLIW PE-to-PE | U.S. 6,446,191 | Pechanek, G Drabenstott, Revilla, J | 09/677,732 |
| 800.0069 | Method and Apparatus for 11/6/2000 Manifold Array Processing | U.S. 6,470,441 | Pechanek, G Pitsianis, N Barry, E | 09/707,209 |
| 800.0071 | Methods and Apparatus for 11/21/2000 Dynamic Very Long Instruction Word Sub-Instruction Selection | U.S. 6,467,036 | Pechanek, G Revilla, J Barry, E | 09/717,992 |
| 800.0072 | Methods and Apparatus for 2/28/2001 Dynamic Instruction Controlled Reconfigurable Regi | U.S. 6,430,677 | Pechanek, G Barry, E | 09/796,037 |

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| 800.0073 | Methods and Apparatus for 10/19/2001 Efficient Vocoder | U.S. | Sadri, A | 10/013,908 |
| 800.0073-PCT | Methods and Apparatus for 10/19/2001 Efficient Vocoder | PCT | Jaffer, N Silivra, A | PCT/US01/45451 |
| 800.0073-EP | Methods and Apparatus for 10/19/2001 Efficient Vocoder | EP | | 01989028.4 |
| 800.0073.PROV | Methods and Apparatus for 10/20/2000 Efficient Vocoder | U.S. | Sadri, A | 60/241,940 |
| 800.0077 | Methods and Apparatus for 12/4/2001 Providing Improved Physical Designs and Routing with Reduc | U.S. | Jaffer, N Silivra, A | 10/004,578 |
| 800.0077.PROV | Methods And Apparatus for 12/4/2000 Providing Improved Physical Designs and Routing with Reduc | U.S. | Chandna, A Brown, D | 60/251,072 |
| 800.0078 | Merged Array Controller with 2/14/2001 Processing Element | U.S. | Chandna, A | 09/783,156 |
| 800.0079 | Methods and Apparatus for 5/14/2001 Providing Direct Memory Access Control | U.S. 6,453,367 | Pechanek, G Revilla, J | 09/854,789 |
| 800.0080 | Methods and Apparatus for 4/25/2002 Pipelined Bus | U.S. | Barry, E | 10/131,941 |
| 800.0080.PROV | Methods and Apparatus for 4/27/2001 Pipelined Bus | U.S. | Wolff, E Baker, D Cope, B | 60/287,270 |
| 800.0081 | Methods and Apparatus to 2/28/2001 Dynamically Reconfigure the Instruction Pipeline of an Ind | U.S. | Wolff, E Baker, D Cope, B | 09/796,040 |
| 800.0088 | Methods and Apparatus for 5/1/2002 Removing Compression Artifacts in Video Sequences | U.S. | Revilla, J Barry, E Marchand, P | 10/136,651 |
| 800.0088.PROV | Methods and Apparatus for 5/4/2001 Removing Compression Artifacts in Video Sequences | U.S. | Petrescu, D | 60/288,965 |

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| 800.0089 | Methods and Apparatus for 10/29/2002 Video Decoding | U.S. | Petrescu, D Stern, T Jacobs, M | 10/282,925 |
| 800.0089.PROV | Methods and Apparatus for 10/30/2001 Video Decoding | U.S. | Petrescu, D Stern, T Jacobs, M | 60/340,620 |
| 800.0093 | Methods and Apparatus for 4/10/2002 Automated Generation of Abbreviated Instruction Set an | U.S. | Larin, S Pechanek, G Conte, T | 10/119,660 |
| 800.0093.PROV | Methods and Apparatus for 4/13/2001 Automated Generation of Abbreviated Instruction Set an | U.S. | Larin, S Pechanek, G Conte, T | 60/283,582 |
| 800.0097 | Methods and Apparatus for a 10/29/2002 Bit Rake Instruction | U.S. | Wolff, E Molnar, P Elezabi, A | 10/282,919 |
| 800.0097.PROV | Methods and Apparatus for a 11/1/2001 Bit Rake Instruction | U.S. | Wolff, E Molnar, P Elezabi, A | 60/335,159 |
| 800.0101 | Methods and Apparatus for 6/29/2001 Providing Data Transfer | U.S. 6,457,073 | Barry, E Wolff, E | 09/896,687 |
| 800.0104 | Methods and Apparatus for 9/28/2001 Scalable Instruction Set Architecture with Dynamic Comp | U.S. | Pechanek, G Barry, E Revilla, J | 09/969,077 |
| 00.0114.PROV | Motion Estimation Method for 4/18/2002 MPEG-4 Simple Profile Video Coding for a MPEG-4 Codec on M | U.S. | Petrescu, D Searles, D | 60/373,551 |
| 800.0119 | Manifold Array Processor 12/21/2001 | U.S. | Pechanek, G | 10/036,789 |
| 800.0121 | Methods and Apparatus for 2/11/2002 Instruction Addressing in Indirect VLIW Processors | U.S. | Barry, E Pechanek, G | 10/073,782 |
| 800.0122 | Methods and Apparatus to 4/1/2002 Support Conditional Execution in a VLIW-Based Array Processo | U.S. | Drabenstott, Pechanek, G Barry, E | 10/114,652 |
| 800.0123 | Methods and Apparatus for 4/1/2002 ManArray PE-PE Switch Control | U.S. | Barry, E Pechanek, G Drabenstott, | 10/114,646 |

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| 800.0125 | Method and Apparatus for 9/24/2002 Manifold Array Processing | U.S. | Pechanek, G Pitsianis, N Barry, E | 10/254,049 |
| 800.0126 | Methods and Apparatus for 9/24/2002 Dynamic Very Long Instruction Word Sub-Instruction Selection | U.S. | Pechanek, G Revilla, J Barry, E | 10/254,012 |
| 800.0127 | Methods and Apparatus for 9/24/2002 Providing Data Transfer | U.S. | Barry, E Wolff, E | 10/254,105 |

Exhibit B

ASSIGNMENT AND TRANSFER OF PATENTS

WHEREAS, Altera Corporation, a Delaware corporation, with offices at 101 Innovation Drive, San Jose, California, 95134 ("Assignor") owns certain patent applications and/or registrations, as listed in Exhibit A attached hereto and incorporated herein by this reference ("Patents"); and

WHEREAS, PTS Corporation, a Delaware corporation, with offices at 101 Innovation Drive, San Jose, California 95134 ("Assignee"), desires to acquire all of the right, title and interest of Assignor in, to and under the Patents;

WHEREAS, Assignor and Assignee have entered into an agreement providing for the assignment of, among other things, all right, title and interest in and to the Patents and in and to the registrations for same from Assignor to Assignee. The parties wish to enter into this assignment to effect the legal and beneficial transfer of all rights in and to the Patents and to fully vest the same in the Assignee;

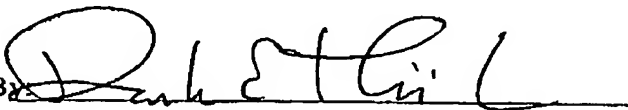
NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Assignor does hereby irrevocably sell, assign, transfer and convey unto Assignee all of its right, title and interest in and to the Patents, including all divisions, continuations, continuations-in-part, reexaminations, substitutions, reissues, extensions and renewals of the applications and registrations for the Patents (and the right to apply for any of the foregoing); all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the Patents throughout the universe, including without limitation all foreign counterparts and foreign equivalents of any of the foregoing.

Assignor authorizes and requests the patent officials in the United States and in any and all foreign jurisdictions to issue any and all letters patent and foreign counterparts or equivalents thereof to PTS Corporation, as assignee of the entire interest of Assignor therein, and covenants that Assignor has full right to convey the entire interest herein assigned and that Assignor has not executed and will not execute any agreements in conflict herewith.

Assignor further agrees, for itself, its successors and assigns, to execute such further documents and to perform such further lawful acts as may reasonably be required to effectuate this assignment.

IN WITNESS WHEREOF, Assignor and Assignee have caused this assignment to be duly executed by an authorized officer to be effective April 7, 2003.

ALTERA CORPORATION

By 

Name: Derek E. Minihane

Title: Director, IP Law and Assistant Secretary

On this 7th day of April 2003, personally appeared Derek Minihane to me known, who, being duly sworn, did depose and say that he/she is the Assistant Secretary of the corporation described in and which executed the foregoing instrument that he/she is duly authorized to execute the foregoing instrument.

STATE OF California

COUNTY OF Santa Clara


Notary Public

